Amendments to the Claims

This listing of claims will replace all prior listings of claims in the application.

Listing of Claims

1. (Currently Amended) An image magnifying circuit~~,~~ designed for horizontally enlarging ~~the~~ image data inputted by sampling for ~~the~~a horizontally enlarged display of an image, said circuit comprising an image memory for storing ~~the~~ inputted image data, a coefficient memory for storing predetermined filter coefficients corresponding to a plurality of magnifications, a non-linear magnification controller for ~~not only~~ outputting ~~the~~an enable signal to read out ~~the~~ corresponding image data from the image memory according to any given magnification set for ~~the~~ n number of equal areas ~~and~~, each area having a width w provided by dividing the image to be displayed ~~into~~by n, ~~number (~~n =being an integer of at least 2, ~~or any larger integer) of equal areas but also for~~and outputting ~~the~~a coefficient selection address to read out ~~the~~a corresponding filter coefficient from the coefficient memory~~,~~ and a filter for filtering the image data read out from the image memory according to the filtering coefficient read out from the coefficient memory ~~but also for~~and outputting ~~the~~ image data processed for enlargement according to any magnification set for each of the n number of areas arranged ~~in~~ horizontally.

2. (Canceled)

3. (Canceled)

4. (Currently Amended) The image magnifying circuit defined in ~~claim 3~~claim 9, wherein the area selection signal generator comprises a dot counter for counting ~~the~~a dot clock,

the dot counter being provided with a load terminal L1 for loading the initial signal as a counted value 1, a coincidence detection circuit for ~~not only~~comparing the counted value of the dot counter with the set area width w or 2 times the set area width w to detect ~~that~~whether they ~~are coincidence~~coincide with each other ~~but also for~~and outputting the detection signal, as a counted value 1, to the load terminal L1 of the dot counter, an up/down counter, which can be reset by the initializing signal, for ~~not only~~counting the dot clock according to the enable signal, which is the detection signal of the coincidence circuit, ~~but also for~~and outputting the counted value as the area selection signal, an up/down controller for ~~not only~~controlling the up/down counter to the up-count mode by outputting ~~the~~an H-level signal when the counted value of the up/down counter has become 0 ~~but also for~~and controlling the up/down counter to the down-count mode according to the detection signal of the coincidence detection circuit after ~~the~~a counted value K of the up/down counter has varied to the value corresponding to the central areas of the image to be displayed~~,~~ and ~~a~~an area width controller for ~~not only for~~outputting the set area width w, as a comparison value, to the coincidence detection circuit in the initial state ~~but also for~~and outputting 2 times the set area width w, as a comparison value, to the coincidence detection circuit when the counted value K of the up/down counter has varied to the value corresponding to the central areas of the image to be displayed.

5. (Currently Amended) The image magnifying circuit defined in ~~claim 3~~claim 9, wherein the magnification parameters m set for the n number of areas are distributed symmetrically with respect to the central areas of the image to be displayed.

6. (Original) The image magnifying circuit defined in claim 5, wherein the magnification parameters m set for the n

number of areas are set to decrease gradually towards the leftmost and rightmost areas from the central areas.

7. (Original) The image magnifying circuit defined in claim 5, wherein the magnification parameters m set for the n number of areas are set to increase gradually towards the leftmost and rightmost areas from the central areas.

8. (New) An image magnifying circuit for horizontally enlarging image data inputted by sampling for a horizontally enlarged display of an image, said circuit comprising an image memory for storing inputted image data, a coefficient memory for storing predetermined filter coefficients corresponding to a plurality of magnifications, a non-linear magnification controller for outputting an enable signal to read out corresponding image data from the image memory according to any given magnification set for n number of equal areas, each area having a width w provided by dividing the image to be displayed by n, n being an integer of at least 2, and outputting a coefficient selection address to read out a corresponding filter coefficient from the coefficient memory and a filter for filtering the image data read out from the image memory according to the filtering coefficient read out from the coefficient memory and outputting image data processed for enlargement according to any magnification set for each of the n number of areas arranged horizontally, wherein the coefficient memory comprises a Read Only Memory for storing the predetermined filter coefficients, a memory controller for reading out the filter coefficients from the Read Only Memory according to a transfer start signal and outputting a coefficient writing address and a Read/Write selection signal, a selector selecting either of the coefficient selection address outputted from the non-linear magnification controller or the coefficient writing address outputted from the memory controller, and a coefficient Random Access Memory for storing the coefficient writing address read

out from the coefficient Read Only Memory according to the coefficient writing address outputted from the selector when the Read/Write selection signal is a Write selection signal and reading out the filter coefficient according to the coefficient selection signal outputted from the selector when the Read/Write selection signal is a Read selection signal.

9. (New) An image magnifying circuit for horizontally enlarging image data inputted by sampling for a horizontally enlarged display of an image, said circuit comprising an image memory for storing inputted image data, a coefficient memory for storing predetermined filter coefficients corresponding to a plurality of magnifications, a non-linear magnification controller for outputting an enable signal to read out corresponding image data from the image memory according to any given magnification set for n number of equal areas, each area having a width w provided by dividing the image by n, n being an integer of at least 2, and outputting a coefficient selection address to read out a corresponding filter coefficient from the coefficient memory and a filter for filtering the image data read out from the image memory according to the filtering coefficient read out from the coefficient memory and outputting image data processed for enlargement according to any magnification set for each of the n number of areas arranged horizontally, wherein the non-linear magnification controller comprises an area selection signal generator for generating an area selection signal for sequentially selecting n number of areas, each having the width w, a first selector for selecting for output a magnification parameter m set for a corresponding area according to the area selection signal generated by the area selection signal generator, m being a positive number no greater than n^2 and the magnification being equivalent to n^2/m, an n-bit adder for receiving, as an input, the magnification parameter m selected by the first selector, an address offset arithmetic-logic unit for calculating the start point of the

coefficient selection address according to the input of the magnification parameter m set for the selection start area of the n number of areas, a second selector selecting for output the calculated value of the address offset arithmetic-logic unit and the sum-data of the adder, a first delayer for delaying the output value of the second selector by one sampling period for output as a coefficient selection address and another input to the adder, a logical sum circuit for outputting a logical sum signal of a carry signal of the adder and an initializing signal, and a second delayer for delaying the output signal of the logical sum circuit by one sampling period for output as an enable signal to the image memory.